AMENDMENTS TO THE SPECIFICATION

Please amend the specification at the paragraphs indicated below such that the paragraphs of the specification at those indicated locations are as follows:

A) The paragraph on page 2, beginning at line 16 and continuing through to line 22:

The complexity of the SISO device is mainly determined by its trellis structure, and the trellis structure is determined by the channel structure (channel memory length, precoder memory length, etc.). Specifically, the complexity of each SISO device is determined predominantly by the number of possible states in the SISO device. For example, each bit in a binary sequence represents two possible states. A SISO device designed to receive the binary sequence should include 2^n states, where n is the number of bits each bit depends upon in the sequence.

B) The paragraph on page 4, beginning at line 28 and continuing through to line 35:

Typically, information for transmission over the communication channel 16 is serially encoded as a bit sequence that carries information (such as picture from digital camera or a text document) from the user's application. As shown, the bit sequence (b_u) is encoded by the encoder 18. Depending on the kind of the Turbo code used, a module 20 known as an interleaver (π) may be needed. The encoded bit sequence ~~(b_u)~~ is shifted or interleaved by the interleaver 20. Then, the interleaved bit sequence (b_i) is precoded by a precoder 24. The resulting encoded and precoded sequence (b_{ic}) is transmitted over the communication channel 16.

C) The paragraph on page 5, beginning at line 28 and continuing through to line 31:

As shown in FIG. 1, the iterative decoder process invokes the entire trellis of the SISO device 28 in each iteration. Thus, during the iterative turbo decoding process, if the SISO device has eight possible states, each iteration adds 8 more layers of complexity to the decoding process.

D) The paragraph beginning at page 5, line 32 and carrying over to page 6, line 7:

The Turbo decoder can be made faster and simpler, with an acceptable ~~drop~~ increase in the Bit-Error-Rate (BER) by implementing the Turbo decoder depicted in FIG. 2. Where possible, for the sake of clarity, the same reference numerals are used to indicate the same components. As with the conventional systems, the communication circuit 34 includes an encoding circuit 12, a decoding circuit 36 and a communicating channel 16 connecting the encoding circuit 12 and the decoding circuit 36. The encoding circuit 18 includes an encoder 18 which encodes (b_u) then passes the encoded sequence (~~b_u~~) through an interleaver 20, which performs a shift operation on the encoded sequence (~~b_u~~) to form a shifted sequence (b_i). The shifted sequence (b_i) is then coded by the precoder 24 and transmitted over the communication channel 16.

E) The paragraph on page 6, beginning at line 27 and continuing through to line 32:

Each SISO device 29, 40 has its own ~~state~~ corresponding set of possible states. SISO device 40 has a much greater impact on the overall complexity of turbo decoder 36 than SISO device 29, because SISO device 40 is located inside the iterative loop, which connects the SISO device 40 and the Turbo decoder 32. Thus, the mathematical model is factored into at least two factors of different complexity, and the simpler factor is implemented as SISO device 40 within the turbo decoder 32.

F) The paragraph on page 7, beginning at line 6 and continuing through to line 19:

The trellis structures of SISO devices 29 and 40 can be selected to maximize the performance gains of the turbo decoder loop. Beginning with a mathematical model of the communication channel 16 with the precoder 24, for example, the communication channel 16 with precoder 24 can be described by the following equation:

$$\frac{1+\alpha_1 D+\alpha_2 D^2+\ldots+\alpha_n D^n}{1\oplus \beta_1 D\oplus \beta_2 D^2\oplus\ldots\oplus\beta_k D^k}$$

where the numerator describes the communication channel's impulse response, and the denominator describes the precoder 24. In this equation, the factor (β) takes values in the binary alphabet (β [[ε]] ε{1,2}), and the symbol (⊕) refers to modulo 2 addition. The factor (D) refers to the delay operator, and the exponent refers to the number of delays in the sequence. The factor[[.]](α) is assumed to be a real number.

G) The paragraph beginning on page 7, line 32 and carrying over to page 8, line 12:

The mathematical model of the channel 16 and the precoder 24 can be factored as follows:

$$\frac{f_1(D)f_2(D)\ldots}{g_1(D)g_2(D)\ldots} \qquad \text{(c)}$$

This factorization can be expressed as follows:

$$\frac{f_1(D)f_2(D)\cdots}{g_1(D)g_2(D)} = F_1(D)F_2(D) \qquad \text{(d)}$$

In forming $F_1(D)$ and $F_2(D)$ in equation (d), any possible combination of the ~~terms~~ factors from the numerator and denominator in equation (c) will work. Generally, $F_1(D)$ determines the trellis structure of SISO device 29, and $F_2(D)$ determines the trellis structure of SISO device 40. Thus, the designer of the decoder circuit should choose F1(D) to be more complex than the subsequent SISO device 40. SISO device 29 can have any size trellis as is made necessary by the model.

H) The paragraph on page 14, beginning at line 18 and continuing through to line 25:

FIG. 7 illustrates the BER versus SNR for an LDPC code used as a Turbo code (same as used in FIG. 4). Here, the mathematical model for the communication channel/precoder is as follows:

$$F_1(D)*F_2(D) = \frac{(1+D)(1-D)^2}{(1\oplus D)}$$

In this instance, the model is factored such that SISO device 40 ~~is factored such that it~~ is a four-state device. As shown in FIG. 7, this factorization results in an SNR loss of over 1dB.

I) The paragraph on page 15, beginning at line 11 and continuing through to line 18:

By simplifying the state-trellis structure of each SISO and by placing one of the simpler SISO devices within the loop, the chip area used by the turbo decoder loop can remain relatively small. Specifically, the entire state-trellis of the SISO within the loop must be ~~re-printed on~~ provided for in the chip circuit for each iteration. Thus, the larger state-trellis within the iterative loop, the more complex the circuit must be. By splitting the factorization into simpler subsets, a simpler SISO with a simpler state-trellis structure can be implemented inside the turbo loop, thereby minimizing the circuit footprint.